

**RANDOM ACCESS MEMORY WITH OPTIONAL COLUMN ADDRESS
STROBE LATENCY OF ONE**

Abstract

A random access memory comprises an array of memory cells, a memory configured to receive data from the array of memory cells, a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory, and a circuit configured to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency signal.